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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/921,022	08/02/2001	Guy Harlan Humphrey	10010504-1	7798

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EXAMINER
NGUYEN, MINH T

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 12/02/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/921,022	HUMPHREY, GUY HARLAN	
	Examiner	Art Unit	
	Minh Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 September 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *16 September 2002* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 9/16/02 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3-4, 7-8 and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 5,036,222, issued to Davis.

As per claim 3, Davis discloses an apparatus (Fig. 3) for reducing the slew rate of transition edges of a digital signal on a node VOUT of an integrated circuit, comprising:

a first switchably conductive device N1 characterized by a first threshold voltage (the voltage which starts to turn ON transistor N1), said first switchably conductive device connected between said node VOUT and a voltage source GND and responsive to a driving signal VIN to

allow current conduction from said voltage source to said node when said driving signal is offset from said voltage source by a voltage substantially equal to and greater than said first threshold voltage and to disallow said current conduction when said driving signal is offset from said voltage source by a voltage less than said first threshold voltage (when VIN changes, VOUT changes, and when VIN changes to a first certain voltage, transistor N1 is ON first, the first threshold voltage is the VIN voltage at this first moment, and when the voltage of VIN is less than this first threshold voltage, the current conduction is disallowed through N1, see column 10, lines 16-36); and

a second switchably conductive device (transistors N3 and P4) characterized by a second threshold voltage (the VIN voltage which start to turn ON transistor N3) greater than said first threshold voltage (column 10, line 35, i.e., two steps or "bifurcated turn on"), said second switchably conductive device connected between said node and said voltage source and responsive to said driving signal to allow current conduction from said voltage source to said node when said driving signal is offset from said voltage source by a voltage substantially equal to and greater than said second threshold voltage and to disallow said current conduction when said driving signal is offset from said voltage source by a voltage less than said second threshold voltage (VIN keeps changing, VOUT also keeps changing accordingly, and when VIN changes to a second certain voltage, transistor N3 is ON, the second threshold voltage is the VIN voltage at this second moment, and when the voltage of VIN is less than this second threshold voltage, the current conduction is disallowed through N3).

As per claim 4, the recited limitation is met because transistors N1 and N3 are FETs.

As per claim 1, this claim is merely a method to operate an apparatus having the structure discussed in claim 3 above, since Davis teaches the circuit, he inherently teaches the method. The recited first and second input signals as a driving signal reads on the signal DATA VIN. The operation of the circuit is clearly explained in claim 3 and in the Davis reference, and therefore, there is no need to repeat here.

As per claim 7, this claim is merely a method to operate an apparatus having the structure discussed in claim 3 above, since Davis teaches the circuit, he inherently teaches the method.

As per claim 8, this claim is merely a method to operate an apparatus having the structure discussed in claim 3 above, since Davis teaches the circuit, he inherently teaches the method wherein the monitoring a level step is performed by transistors N1, N3 and P4, i.e., using the difference voltage levels of VIN to turn on transistors N1 and N3 as discussed in claim 3 above as the first and second threshold voltages, when the level of the driving voltage is lower than the monitor level threshold voltage, do not conduct, when the level of the driving voltage is equal or higher, perform the conducting function; the stepping up conduction of current to the node VOUT step when the level reaches a first threshold voltage is performed by transistor N1, and the stepping up conduction of current to the node step when the level reaches a next threshold voltage is performed by transistors N3 and P4.

As per claim 10, Davis discloses a method for controlling the slew rate of transition edges of a digital signal on a node VOUT of an integrated circuit (Fig. 3), the method comprising the steps of:

monitoring a level of a driving voltage (use the threshold voltages which turn off transistors P1 and P3 as first and second threshold levels);

when the level reaches a first threshold voltage, stepping down conduction of current to said node VOUT (gradually turn off the conduction of transistor P1);

when the level reaches a next predefined threshold voltage (the second threshold level), stepping down conduction of current of said node (gradually turn off the conduction of transistor P3).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 5-6, 9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,036,222, issued to Davis in view of US Patent No. 5,877,647, issued to Vajapey et al.

As per claim 5, Davis teaches an apparatus (Fig. 3) for reducing the slew rate of a digital signal which comprises first and second switchably conductive devices having first and second threshold voltages as discussed in claim 3 above but he does not explicitly teach an apparatus which comprises one or more additional switchably conductive devices wherein each has different threshold voltage as called for in the claim.

Vajapey discloses an apparatus (Fig. 6) for controlling the slew rate of an output signal using switchably conductive devices P1 and P2, and in column 7, lines 1-5, he explicitly suggests

another embodiment which has one or more additional switchably conductive devices to further control the slew rate of the digital signal at the node.

It would have been obvious to one skilled in the art at the time of the invention was made to add one or more switchably conductive devices to the Davis's circuit wherein each has different threshold voltage.

The motivation/suggestion for doing so would have been obvious for the reason discussed herein above, i.e., more control of the slew rate of the digital signal at the node VOUT of the Davis's circuit.

Therefore, it would have been obvious to add one or more additional switchably conductive devices to the Davis's circuit shown in Fig. 3 to obtain the invention specified in the claim.

As to the functional limitation recited on lines 7-12 of the claim, the combination discussed herein above clearly functioned as recited.

As per claim 6, the recited limitation is met because the first, second and one or more additional switchably conductive devices are NMOS transistors.

As per claim 2, this claim is rejected for the same reasons noted in claim 5.

As per claim 9, this claim is rejected for the same reason noted in claim 5 wherein the recited stepping up step for one or more additional next predefined threshold voltages are performed by the one or more additional transistors as discussed in claim 5.

As per claim 11, this claim is rejected for the same reason noted in claim 5 wherein the recited stepping down step for one or more additional next predefined threshold voltages are performed by the one or more additional transistors as discussed in claim 5.

Response to Arguments

4. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Nguyen whose telephone number is 703-306-9179. The examiner can normally be reached on Monday - Thursday 7:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 703-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Minh Nguyen
Examiner
Art Unit 2816

MN
November 29, 2002